Code No: A5502, A5702 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, April/MAY-2012
VLSI TECHNOLOGY AND DESIGN
(COMMON TO EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

\- - -

1. Design BiCMOS inverter with neat sketches and explain.

2. Explain Latch –up problem in CMOS circuits and discuss reducing methods.

3. Design a CMOS layout circuit for the function Y=((A+B).C.)'?

4. Calculate K,H,50% delay of the Buffers required when a minimum size inverter drives a metal 1 Wire that is 200 λ ∗3 λ in this case ,Ro=4.9kΩ and Co=0.69fF while Rint=5.34Ω and cint=15fF+90.1fF=105.1fF.

5. Explain in detail about logic & Inter connect Designs with examples.

6. Explain LSSD with Latch example.

7.a) How ASAP & ALAP schedules are differ with data flow graph?
b) Write any one of architectural method for reducing power consumption.

8. Explain a simple Dog Leg routing algorithm.

****